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ORGANIZATION OF DIRECT MEMORY ACCESS

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Abstract:
The work considers the mode of direct access to memory with the provision of communication between the PDP controller and the microcomputer memory. The PDP controller is shown for inputting data from the VU in the "Cycle Capture" mode and disconnecting the processor from the system interface buses.

Keywords: organization, direct, memory, access, provision, capture, cycle, processor, controller.

Introduction

One of the methods of data exchange with the CU is exchange in the direct memory access (DMA) mode. In this mode, data exchange between the CU and the main memory of the microcomputer occurs without the participation of the processor. Exchange in the DMA mode is controlled not by the program executed by the processor, but by electronic circuits external to the processor. Usually, the circuits controlling the exchange in the DMA mode are located either in a special controller, which is called a direct memory access controller, or in the controller of the CU itself.

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Data exchange in the PDP mode allows the use of high-speed external storage devices in microcomputers , such as hard disk drives, since the PDP can provide the time for exchanging one byte of data between the memory and the storage device equal to the memory access cycle.

To implement the direct memory access mode, it is necessary to provide a direct connection between the PDA controller and the microcomputer memory . For this purpose, it would be possible to use specially allocated address and data buses connecting the PDA controller with the main memory. But such a solution cannot be considered optimal, since it will lead to a significant complication of the microcomputer as a whole, especially when connecting several VPUs. In order to reduce the number of lines in the microcomputer buses, the PDA controller is connected to the memory via the address and data buses of the system interface. This raises the problem of joint use of the system interface buses by the processor and the PDA controller. Two main ways to solve it can be distinguished: implementation of exchange in the PDA mode with "cycle capture" and in the PDA mode with processor locking.

There are two types of direct memory access with "cycle capture". The simplest way to organize DMA is that those machine cycles of the processor are used for exchange, in which it does not exchange data with memory. In such cycles, the DMA controller can exchange data with memory without interfering with the processor operation. However, it is necessary to select such cycles so that there is no temporary overlap of DMA exchange with exchange operations initiated by the processor. In some processors, a special control signal is generated, indicating cycles in which the processor does not access the system interface. When using other processors, to select such cycles, it is necessary to use special selecting circuits in the DMA controllers, which complicates their design. The use of the considered method of DMA organization does not reduce the performance of the microcomputer , but at the same time, exchange in the DMA mode is possible only at random moments of time with single bytes or words.

More common is the DMA with "cycle capture" and forced disconnection of the processor from the system interface buses. To implement this DMA mode, the microcomputer system interface is supplemented with two lines for transmitting control signals "Request for direct memory access" (RDMA) and "Granting direct memory access" (GDMA).

The TPDA control signal is generated by the direct memory access controller. The processor, having received this signal, suspends the execution of the next command without waiting for its completion, issues the PPDA control signal to the system interface and disconnects from the system interface buses. From this moment on, all system interface buses are controlled by the TPDA controller. The TPDA controller, using the system interface buses, exchanges one byte or word of data with the microcomputer memory and then, having removed the TPDA signal, returns control of the system interface to the processor. As soon as the TPDA controller is ready to exchange the next byte, it again "captures" the processor cycle, etc. In the intervals between TPDA signals, the processor continues to execute program commands. Thus, program execution slows down, but to a lesser extent than during exchange in interrupt mode.
The use of data exchange with the CU in the PDP mode in a microcomputer always requires preliminary preparation, namely: for each CU it is necessary to allocate a memory area used for the exchange and specify its size, i.e. the number of bytes (words) of information written to or read from the memory. Consequently, the PDP controller must necessarily have an address register and a byte (word) counter. Before starting the exchange with the CU in the PDP mode, the processor must execute the loading program. This program ensures that the initial address of the memory allocated to the CU and its size in bytes or words is written to the specified registers of the PDP controller, depending on what portions of information are being exchanged. The above does not apply to the initial loading of programs into the memory in the PDP mode. In this case, the contents of the address register and the byte-word counter are set by switches or jumpers directly on the controller board.
The block diagram of a simple PDP controller that provides data input into the microcomputer memory at the initiative of the control unit in the “Cycle Capture” PDP mode is shown in Fig. 3.17.

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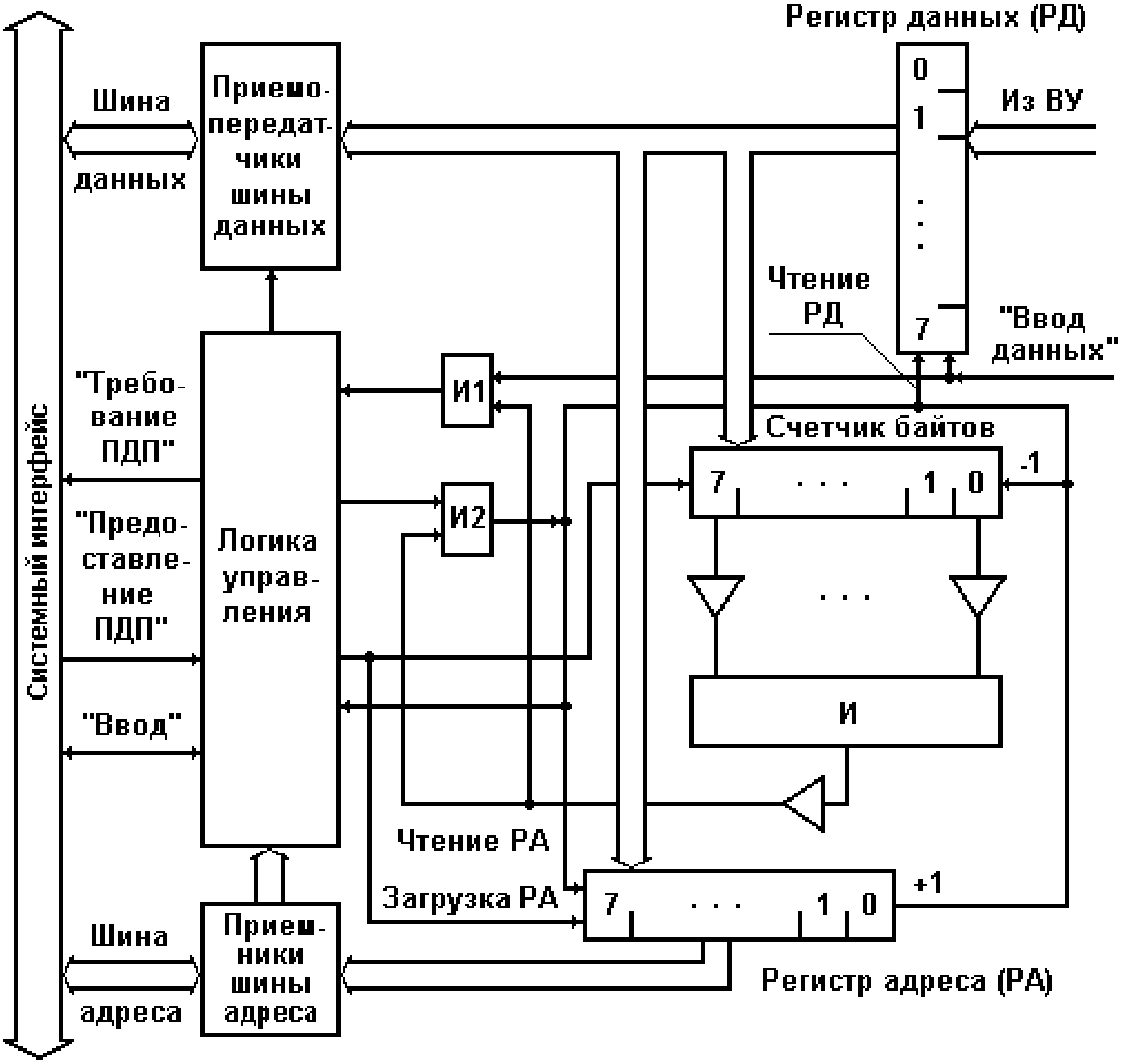

Fig. 1 - PDP controller for data input from the VU in the "Cycle Capture" mode and disconnecting the processor from the system interface buses

Before the start of the next data input session from the VU, the processor loads the following information into the registers of its controller: into the byte counter - the number of bytes of data received, and into the address register - the starting address of the memory area for the input data. Thus, the controller is prepared to perform the operation of inputting data from the VU into the microcomputer memory in the PDP mode.

The data bytes from the CU enter the controller data register at a constant rate. In this case, each byte is accompanied by a control signal from the CU "Data Input", which ensures that the data byte is written to the controller data register. Based on the same signal and with a non-zero state of the byte counter, the controller generates a TPDP signal. Based on the response signal from the PPDP processor, the controller sets the contents of its address and data registers to the address and data buses of the system interface, respectively. By generating the "Output" control signal, the PDP controller ensures that the data byte is written from its data register to the microcomputer memory . The PPDP signal is used in the controller to modify the byte counter and the address register. Based on each PPDP signal, one is subtracted from the contents of the byte counter, and as soon as the contents of the counter become zero, the controller stops generating "Direct Memory Access Request" signals.

Using the example of a simple PDP controller, we have considered only the process of preparing the controller and directly transferring data in the PDP mode. In practice, any session of data exchange with the CU in the PDP mode is always initiated by a program executed by the processor and includes the following two stages.

1. At the stage of preparing the CU for the next exchange session, the processor in the program-controlled exchange mode polls the CU state (checks its readiness for exchange) and sends commands to the CU that ensure the preparation of the CU for exchange. Such preparation can be reduced, for example, to moving the heads to the required track in the hard disk drive. Then the registers of the PDP controller are loaded. At this point, preparation for exchange in the PDP mode is completed and the processor switches to executing another program.

2. Data exchange in the PDP mode begins after the completion of preparatory operations in the CU, at the initiative of either the CU, as discussed above, or the processor. In this case, the PDP controller must be supplemented with a status and control register, the contents of which will determine the operating mode of the PDP controller. One of the bits of this register will initiate data exchange with the VU. Loading information into the status and control register of the PDP controller is performed programmatically.

The most common is the exchange in the direct memory access mode with the processor lock. It differs from the DMA with "cycle capture" in that the control of the system interface is transferred to the DMA controller not for the time of exchange of one byte, but for the time of exchange of a data block. This DMA mode is used in cases where the time of exchange of one byte with the CU is comparable with the cycle of the system bus.

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In a microcomputer, it is possible to use several CUs operating in the PDP mode. Provision of such CUs with system interface buses for data exchange is performed on a priority basis. The priorities of the CUs are implemented in the same way as during data exchange in the interrupt mode, but instead of the control signals "Interruption request" and "Interruption grant" (Fig. 18 Organization of interrupts in a microcomputer), the signals "Direct access request" and "Direct access grant" are used, respectively.

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